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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,943	02/26/2004	Mitrajit Chatterjee	IDT-1872	6684

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2117	

MAIL DATE	DELIVERY MODE
08/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

SUPPLEMENTAL

Office Action Summary

Application No.	Applicant(s)	
10/788,943	CHATTERJEE ET AL.	
Examiner	**Art Unit**	
JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH([redacted]) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/20/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16,18-25 and 27-40* is/are pending in the application.

4a) Of the above claim(s) *32-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,18-25,27-31 and 38-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

SUPPLEMENTAL ACTION

This is a Supplemental Office Action responsive to amendment after final, filed 8/20/2007 and supplemental to the Final Office Action mailed 8/20/2007.

In response to Applicant's assertion that the Final Office Action mailed on June 20, 2007 that the rejection of independent claim 25 is improper for failing to fully address the claimed limitations in the claim, the Examiner has withdrawn the rejection of claim 25, and a new rejection of claim 25 is set forth in the Supplemental Office Action, under the same grounds 35 U.S.C § 103(a) as being unpatentable over Koschella (U.S. Patent No. 7,054,121) in view of Desmicht et al. (US 20060156033), for the purpose of further clarifying the rejection of the claimed limitations of the Final Office Action.

Response to Arguments

Applicant's arguments filed 8/20/2007, with respect to claim 25, have been fully considered but they are not persuasive.

Applicant's argument that neither interface or Desmicht describe "a JTAG interface clocked by a JTAG clock signal received from an external JTAG hardware", as recited in claim 25, is not persuasive, because Koschella discloses an externally accessible data interface 6, which is a standard Joint Test Action Group (JTAG) interface. According to Koschella, the data can also be read as data d1 at the externally accessible data interface 6 or written from there into the memory device 3, Fig. 1. Even though, Koschella does not show a JTAG clock signal, a person of ordinary skill in the art is well aware that a JTAG clock signal (TCK) is inherently part of JTAG IEEE

Standard 1149.1 signals including (TMS, TCK, TDI, and TDO), which are normally provided from an external test system compliant with standard IEEE 1149.1 JTAG interface.

In response to Applicant's argument that neither Koschella or Desmicht describe the claimed limitations of "a controller configured to allow said external JTAG hardware to write information into said non-volatile memory through said JTAG interface, wherein said controller is clocked either by a system clock signal or by said JTAG clock signal if said system clock signal is not available", as recited in claim 25, Koschella discloses (logic device 5.1) Figs. 4 and 6, which allows the external test system compliant with standard IEEE 1149.1 JTAG interface to write (data d1) into the memory device 3. The controller is clocked by a system clock signal write clock, which is a register write enable signal WE_{MPCR} from the CPU 2, which generates the read enable signal $RE_{memory\ i}$ or write enable signal $WE_{memory\ i}$, respectively, for reading or writing in the selected memory area, Fig. 6.

The recited limitation "or by said JTAG clock signal if said system clock signal is not available" is in the alternative format, and therefore it has not been given patentable consideration. In this case, only the limitation "said controller is clocked by a system clock signal" has been given patentable consideration, as described above.

Assuming arguendo, the controller is clocked by the JTAG clock signal, Koschella discloses JTAG signals coupled the inputs of the AND gate 14, which include a (TCK) clock for clocking the controller, as shown in Fig. 6.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koschella (US-Patent No. 7,054,121) in view of Desmicht et al. (US 20060156033).

Regarding independent Claim 25, Koschella discloses a processor-memory system with a protection circuit, Fig. 1, comprising:

A memory (memory device 3) including a protected area (B0, B1,Bi,. . Bn), which is protected by a protection circuit 1, in the event of an unauthorized external memory access.

"a JTAG interface clocked by a JTAG clock signal received from an external JTAG hardware", such as an externally accessible data interface 6, which is a standard Joint Test Action Group (JTAG) interface. The data can also be read as data d1 at the externally accessible data interface 6 or written from there into the memory device 3, Fig. 1. A JTAG clock signal (TCK) is inherently part of JTAG IEEE Standard 1149.1 signals including (TMS, TCK, TDI, and TDO), which are normally provided from an external test system compliant with standard IEEE 1149.1 JTAG interface.

"a controller configured to allow said external JTAG hardware to write information into said non-volatile memory through said JTAG interface, wherein said controller is clocked either by a system clock signal or by said JTAG clock signal if said system clock signal is not available", such as (logic device 5.1) Figs. 4 and 6, which allows the external test system compliant with standard IEEE 1149.1 JTAG interface to write (data d1) into the memory device 3. The controller is clocked by a system clock signal write clock, which is a register write enable signal WE_{MPCR} from the CPU 2, which generates the read enable signal $RE_{memory\ i}$ or write enable signal $WE_{memory\ i}$, respectively, for reading or writing in the selected memory area, Fig. 6.

The recited limitation "or by said JTAG clock signal if said system clock signal is not available" is in the alternative format, and therefore it has not been given patentable consideration. In this case, only the limitation "said controller is clocked by a system clock signal" has been given patentable consideration, as described above.

Nevertheless, even if "the controller is clocked by the JTAG clock signal", Koschella discloses JTAG signals coupled the inputs of the AND gate 14, which include a (TCK) clock for clocking the controller, as shown in Fig. 6.

Koschella discloses a processor-memory system with a protection circuit, Fig. 1, having memory device 3, which is integrated wholly or in part with the microcontroller, or forms a separate physical unit depending on the type of microcontroller and the amount of memory required.

Koschella fails to disclose that the memory device in a non-volatile memory. However, the memory device may be implemented as a non-volatile memory, since

there is nothing distinctly unique feature in a non-volatile memory that precludes the protection circuit disclosed by Koschella to operate properly with a microcontroller and a non-volatile memory.

In analogous art, Desmicht et al. (US 20060156033) discloses, Fig. 2, a chip CHP that includes a non-volatile memory NVM, including protection data ADA and protected data PDA, the protection data being intended to be used for authorizing or denying access to the protected data PDA by the microprocessor MP under the execution of a program PRO. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a non-volatile memory NVM as taught by Desmicht, in Koschella's processor-memory system, since non-volatile memories are more secure in maintaining the integrity of protected data, especially during power interruptions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Date: 23 August 2007
Office Action: Supplemental Action

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8/23/07

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